Temporary Wafer Bonding Materials and Processes

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Abstract:

Recent years have seen significant advances in temporary wafer bonding with materials providers seeking to meet the growing demands of 2.5D and 3D applications. Many types of temporary bonding solutions have been developed that use different methodologies for bond and de-bond. We have examined four different types of temporary wafer bonding materials for use in two separate applications: a face-up, stackable 3D-IC application with TSVs and backside Cu/Sn interconnects, and a silicon interposer with large TSVs, polymer dielectrics, and solder balls. We present results of the fabrication of these two types of test vehicles and discuss the compatibility of the process flows with the temporary wafer bonding materials. For the 3D-IC application, 15 μm thin silicon wafers on three different temporary bond materials were processed through BEOL processes for the passivation, electroplating, and bonding of Cu/Sn microbumps. For the silicon interposer application, results will be reported from a test vehicle lot on the compatibility of two different temporary bond materials with three photoimageable polymer dielectrics and with the process for bumping and de-bonding.

1. Introduction

Temporary wafer bonding has been used for many years to provide mechanical support to device wafers during thinning processes. However, the advent of 2.5D and 3D integration is placing significantly higher demands on the performance of temporary bonding materials as more fabrication processes are required on progressively thinner wafers [1-4]. In response, materials providers have recently developed several different types of temporary bonding solutions that seek to provide a robust carrier with a simple debond process [5, 6]. Table 1 lists some of the common temporary bond materials available and gives their methodology for bonding and debonding. In general, recent developments have focused on room temperature bonding.

Typical 2.5D or 3D integration process flows will require more than just backgrinding and CMP to be done on the backside of thinned wafers. RIE, PECVD oxide deposition, lithography, and electroplating are generally required to complete the TSV interconnects. Each of these operations, and the order in which they are sequenced, will impose certain requirements on the temporary bond material, as several groups have reported [7-9]. In this paper, ongoing work at RTI to evaluate temporary bond materials for silicon interposer and 3D-IC applications will be presented. In this context, different categories of available temporary wafer bonding solutions will be examined with regard to their bonding and debonding details as well as their resistance to, and compatibility with, various BEOL operations.

Table 1. Temporary Wafer Bonding Solutions

Company	Material	Bonding	Carrier	Debond	Debond Temp (°C)	Equipment
3M	Acrylic adh	UV	glass	YAG laser	RT On flex frame	Suss, Tazmo
Brewer	thermoplastic	thermal	Si / glass	Thermal slide	180	EVG, Suss
Brewer (Zonebond®)	thermoplastic	thermal	Si / glass	solvent	RT	EVG, Suss
DuPont	PI	thermal	glass	Excimer laser	RT On flex frame	Suss
TMAT	Silicone elastomer	thermal	Si / glass	mechanical	RT On flex frame	Suss
TOK	NA	thermal	glass	solvent	RT	TOK

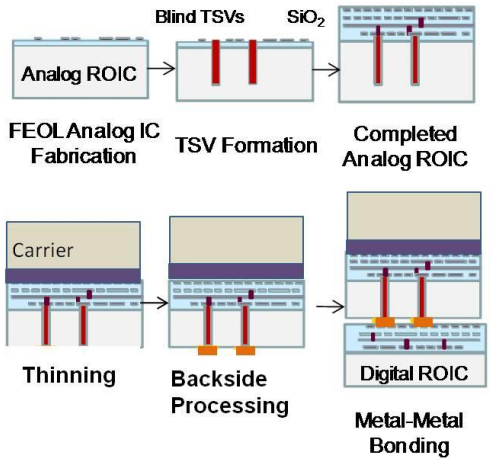

Figure 1. Process flow for the fabrication of a stackable 3D-IC using a temporary carrier.

2. Fabrication and Discussion

A. Temporary Wafer Bonding for 3D-IC

Work at RTI has focused on evaluating temporary wafer bond materials for two different process flows. The first, shown in Figure 1, is the fabrication of TSVs and backside interconnects for a face-up, stackable 3D-IC application. Here the TSVs are etched and filled, then connected to the top metal levels while the wafer is full thickness. The wafer is then bonded to a support and thinned to reveal the TSVs. In this sequence, the temporary bond material must be compatible with the process steps needed to repassivate the TSVs and form microbumps on the wafer backside, which include RIE of silicon and oxide, PECVD oxide deposition, CMP, lithography, electroplating, and wet etching or ion milling. For these tests, 150 mm diameter SOI wafers with 3 μm diameter and 15 μm deep copper TSVs and 200 mm diameter silicon wafers without TSVs were bonded with Nitto Denko Revalpha thermal release tape, Thin Materials AG (TMAT) silicone elastomer adhesive, and thermoplastic WaferBOND® 9001 from Brewer Science. Table 2 lists the observed compatibility of these three materials with the processes required for a stackable 3D-IC application. To create die that could be bonded on RTI's SET FC150 without special precautions for thin die handling, the thin wafers were diced while on the carrier. Debonding of the carrier wafer was done at the die level, after the thin die was bonded to a substrate. For the wafers supported with WaferBOND no special dicing precautions needed to be used. For Revalpha and TMAT wafers an extra process level was required to etch the thin silicon

Table 2. Compatibility chart for four different categories of temporary bond materials and 3D-IC process sequences

Temporary Bond Type	Thinning	Backside Process	Dicing on Carrier	Die Bonding & Release
Thermal Release Tape	Good	Solvent susceptible	Poor	< 200 C bonding only
Thermoplastic	Good	Good	Good	Flows during bonding
Mechanical Release	Good	Good	Special dicing conditions	Good

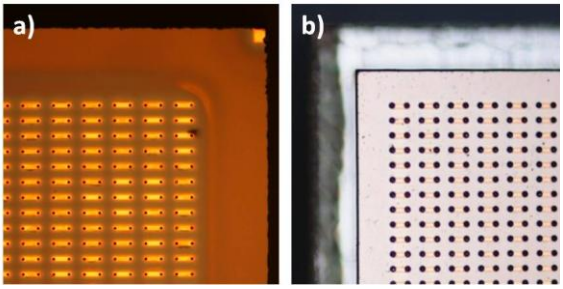

Figure 2. Diced edges of 15 um thin die on a) WaferBOND 9001 and b) TMAT. The thin silicon was removed by RIE from the dicing streets in b).

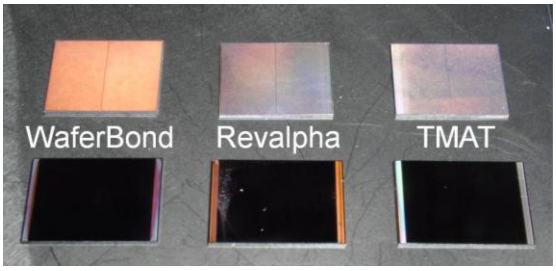

Figure 3. Images of thin die on three different carriers (top row) and thin die bonded to full thickness die (bottom row, shown after carrier removal). Residue from removal of the Revalpha carrier is visible on the bottom center die.

from the dicing streets before dicing the carrier. Figure 2 shows images of the diced edges from two representative die. Both TMAT and WaferBOND supported die showed 99.99% bond yield and clean release of the carrier after bonding at 250 C for 180 s using solid–liquid Cu/Sn – Cu diffusion bonding [10]. Figure 3 shows images of thin die on the three different temporary bond materials before die bonding and after bonding and release of the carrier. WaferBOND was observed to flow and squeeze out during bonding. While this squeeze out did not affect bond yield around the perimeter of the die, further work is needed to determine compatibility with a pre-dispensed underfill.

B. Temporary Wafer Bonding for Silicon Interposer

The second process flow for which temporary wafer bonding materials are being characterized at

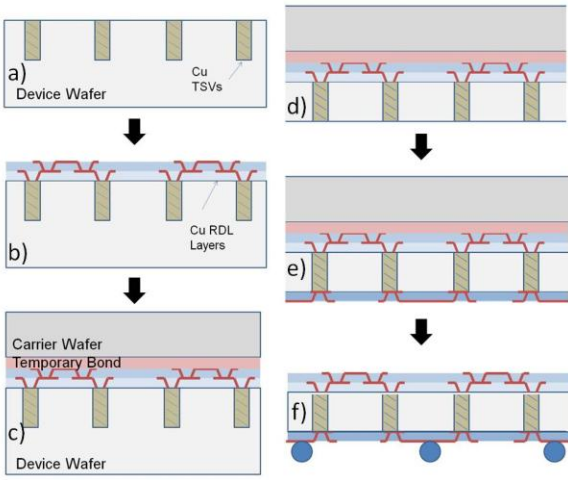

Figure 4. Process flow for fabrication of the silicon interposer test vehicle

RTI is the fabrication of silicon interposer die with large 25 µm diameter and 100 µm deep copper filled TSVs, backside RDL with spin-on dielectric materials, and 125 µm solder bumps, as shown in Figure 4. For this application a temporary wafer bonding material must be able to support the target wafer through thinning, backside dielectric lithography, polymer curing, and solder reflow. In some scenarios, the temporary carrier will then be diced and will support the thin die through solder bump bonding. In other scenarios, the temporary carrier will be debonded from the thinned wafer before dicing.

WaferBOND 9001 and 3M's Wafer Support System (WSS) were chosen as the temporary bond materials for the silicon interposer demonstration lots. For logistical reasons TMAT was not included in these tests though it is an attractive candidate due to its rigidity at the temperatures needed for curing common spin-on dielectrics. The spin-on dielectrics chosen for the backside passivation layers were BCB 4024-40 (Dow Chemical), HD-8930 (polybenzobisoxazole [PBO] HD Microsystems), and the fluorinated aromatic AL-X 2010 (Asahi Glass Corp.). The cure temperatures of these three materials are 250˚C, 200˚C, and 190˚C, respectively; all below the given temperature limit of the temporary bond materials. The first interposer demonstration lot consists of 150 mm diameter wafers, without TSVs, split in a test matrix of the two temporary bond materials and three dielectric materials. The front side of the wafers was patterned with two levels of copper RDL and two levels of polyimide passivation. After front side patterning, the wafers were bonded and thinned to 100 µm. Final polish was done at Entrepix, Inc. TTV data

Table 3. TTV of thin wafers on different temporary bond materials

Wafer Number	Wafer Diameter	Wafer TTV PreThin	Adhesive Thickness	Wafer TTV Post Thin
	(mm)	(um)	(um)	(um)
9001-1	150	2.1	nominally 30	1.0
2	150	5.1		3.7
3	150	2.9		2.3
4	150	2.7		2.8
5	150	2.5		2.5
3M WSS-1	150	3.2	47.5	2.5
2	150	3.2	49	2.0
3	150	6.4	48.1	2.7
4	150	2.9	51.1	2.7
5	150	3.5	52.6	3.7
6	150	2.5	51.2	3.9
TMAT-1	200	6.56	53.39	8.01
2	200	6.13	47.19	4.6
3	200	4.77	31.02	4.06

from the device wafers pre- and post thinning is shown in Table 3, along with data taken from 200 mm diameter wafers on TMAT. None of the three materials contributed significantly to the final TTV. After thinning, the wafers were coated and patterned with a dielectric material and cured. No delamination or blistering of the thinned wafer was observed in any of the six combinations of bond and dielectric materials. All three WaferBOND wafers exhibited some slight bubbles in the exposed material around the edge of the carrier that solidified and created standoffs between the wafers and the photomasks used for lithography of the subsequent layers. However, this did not limit the resolution needed for the next process level, and it is expected that the bubbles could easily be removed if necessary using the recommended stripper.

After completion of the backside RDL level, 125 µm tall eutectic Sn-Ag solder bumps were electroplated on the wafers and reflowed at 240˚C. The seed layer was removed by wet etching. Completed interposer test wafers on WaferBOND and 3M WSS are shown in Figure 5.

Two process flows are under evaluation for de-bonding of the silicon interposer test wafers. The WaferBOND wafers will be diced while on the carrier, the thin silicon die bonded to a substrate, and the carrier will be removed. The carrier removal can be done either through a solvent release or by heating the carrier below the melting point of the Sn-Ag bumps and sliding off. The addition of memory or logic chips to the front side of the interposer would have to be done before the temporary bond while the interposer was full thickness or after removal of the

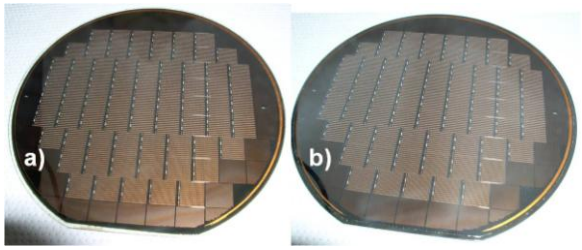

Figure 5. Interposer test wafers after completion of backside processing and bumping on a) 3M WSS and b) WaferBOND 9001 carrier wafers

carrier following solder bonding and underfill. For the wafers bonded with 3M WSS a second carrier wafer will be attached to the bumped side of the target wafer. This will allow the first carrier to be removed and the thinned wafer to be debonded, front side down, onto a dicing frame. In this manner the thin wafer is fully supported during the dicing operation, as opposed to being supported only at the solder bumps. The second carrier process also allows access to the front side of the interposer for possible bonding of memory and logic chips prior to dicing.

3. Conclusion

RTI has been evaluating several temporary wafer bonding solutions for 3D-IC and silicon interposer applications. A 15 μm thin, stackable 3D-IC test vehicle with area array TSVs and Cu-Sn interconnects on a 10 μm pitch was successfully fabricated, bonded, and released using both WaferBOND 9001 and TMAT temporary bonding materials. Both these materials provided rigid support to thinned wafers through the backside processes needed for the passivation and formation of Cu-Sn interconnects, as well as supporting the thin wafer in dicing and bonding operations. Differences in the behavior of these materials during dicing and bonding were noted that could have an effect on certain applications.

An evaluation of temporary bond materials for fabrication of a 100 μm thick silicon interposer with backside RDL, polymer dielectrics, and solder bumps was also shown. 3M's WSS and WaferBOND 9001 were used to support thin wafers through the curing of BCB, PBO, and AL-X spin-on dielectric materials. No degradation or impact on subsequent lithography steps was observed. Finally, possible process sequences were discussed for the dicing and de-bonding of the silicon interposer test wafers and their integration in a system.

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