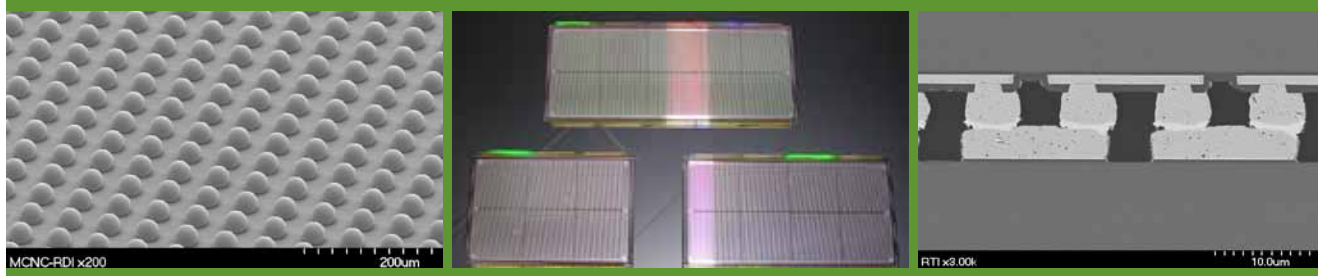


MICROSYSTEM INTEGRATION AND PACKAGING

Advanced Interconnect and Packaging Technologies

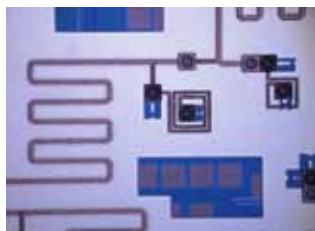


RTI International is home to one of the premier wafer bumping and wafer level packaging research and fabrication facilities in the U.S. Our experts in material and electronic technologies have over 15 years of research, development, and implementation experience in all areas of bump interconnect technologies. From material characterization, to prototype and proof of concept, to pilot-line and small-scale production, we tailor our capabilities to meet each client's unique requirements.

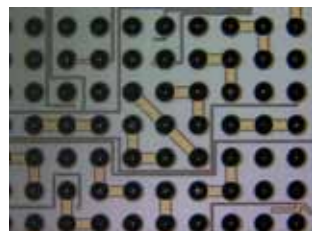
Solder Bumping and Wafer Level Chip Scale Packaging

RTI International is a world leader in advanced interconnect and packaging technologies. RTI provides access to state-of-the-art wafer bumping and wafer level packaging (WLP) technologies, supporting small- and mid-volume customers as well as developmental applications. Services and processes we offer include:

- Bump on I/O Pad
- Bump on Polymer
- Polymer Repassivation
- Single and multiple layer redistribution
- Eutectic Sn/Pb, Pb-free, and Cu pillar bumping
- Design services



Multi-layer BCB and Cu redistribution



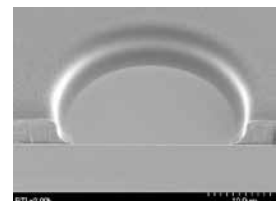
Electroplated and ball drop bumping processes

Clients can take advantage of our standard repassivation, redistribution, and bumping processes, or we can customize the processes and materials used for your specific application.

If you're thinking about evaluating new structures and materials for your applications, RTI can help with design, fabrication, testing, and analysis. Our flexibility coupled with our extensive engineering knowledge in wafer bumping and WLP technologies makes RTI the ideal partner for your development needs.

Electronic Material Characterization and Process Development

RTI's extensive experience in flip chip and WLP makes us an ideal development partner for suppliers of electronic materials. Our capabilities allow us to provide a full spectrum of services for evaluating new materials, from basic characterization and process parameterization to full implementation into WLP structures, reliability testing, and analysis. We help you learn how your material performs in the processes your customers use, and we



Evaluation and characterization of new electronic materials for advanced interconnect

can work collaboratively with you and your customers to develop new processes unique to your materials. With state-of-the-art equipment and end-to-end process support, RTI can help you evaluate your products and get them into your client's hands more quickly.

Ultra-Fine Pitch Flip Chip Bumping

RTI is a world leader in ultra-fine pitch flip chip technology, and our standard 50 micron I/O pitch process enables an interconnect density of 40,000 I/O per cm². Originally developed for advanced multichip module technologies in the 1990s, this technology has been used extensively in bumping pixelated particle detectors for high energy physics applications. Several hundred 50 micron pitch devices have been installed at CERN in experimental apparatus used at the Large Hadron Collider. Ideally suited for mating Si-to-Si devices, this process has also found applications in other advanced imaging, optoelectronic, and IC applications.



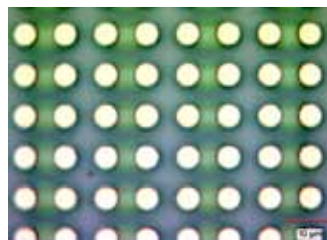
*25 micron diameter bumps
on 50 micron pitch*

Flip Chip and Multichip Module Assembly

RTI also offers flip chip assembly – from single chip placements to multichip module and system-in-package assembly of multiple die and components. Assembly is performed in a controlled environment for reduced particulate contamination. Our patented plasma-assisted dry soldering (PADS) process is a revolutionary technology that allows soldering to be done without the use of flux. Recognized with an R&D 100 award, PADS has been successfully used in board-level soldering assembly as well as in flip chip applications. PADS is an integral part of fine-pitch flip chip assembly, where large chip area and small standoff height make flux residue removal very difficult. The use of PADS is also advantageous in the assembly of MEMS and optoelectronic devices, where the use of flux can damage the operation of such devices.

Metal-Metal Bonding for 3D Integration

Rising interest in 3D integration technology is resulting in a need for extremely high interconnect densities for chip stacking and high I/O devices. RTI is a leader in the development and implementation of metal-metal bonding technologies, with proven technologies for fabricating and bonding CuSn-Cu and Cu-Cu full-area bump arrays with pitches as small as 10 microns. The resulting interconnect array is extremely strong mechanically and thermally stable at temperatures well above the thermal budget of most IC devices (> 400C). These interconnect structures can be applied to most IC wafers for high I/O density interconnection, chip stacking for 3D integration, Si-to-Si integration, and applications requiring thermal and mechanical stability at temperatures beyond that of typical solder materials.



*Array of Cu bumps
at 10 micron pitch*

Working with RTI

RTI is a not-for-profit company and ITAR registered organization that offers a “safe harbor” development environment to its clients. We work with a diverse base of commercial clients, government agencies, and academic institutions, supporting our clients through application-driven technology development programs, custom prototyping, and small volume production. We also partner with external organizations for joint proposals in a variety of government and defense programs (classified and unclassified), including SBIR and STTR programs.

More Information

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