

MICROSYSTEM INTEGRATION AND PACKAGING

3D Integration Technology

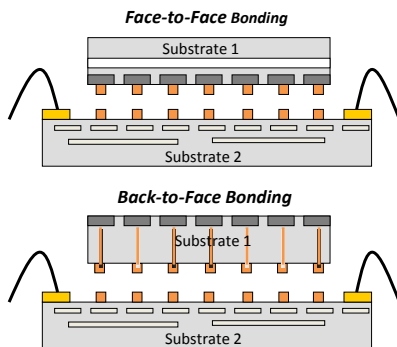


RTI International is a leader in 3D integration technology, having developed a wide range of 3D process capabilities and achieved successful demonstrations of 3D integrated IC stacks, advanced Si interposer wafers, and 3D passive device structures. In one such illustration, RTI demonstrated, in collaboration with a major U.S. defense contractor, the first mixed-signal 3D integrated bulk CMOS IC stack for infrared imaging applications. RTI has been conducting research and development in 3D integration since 1999, building on decades of experience in the development of advanced microfabrication and packaging technologies.

RTI works with a wide variety of clients and partners, bringing integrated process, design, testing, and analysis capabilities to projects involving custom application-driven development. RTI is offering access to its 3D technology platform through joint development projects, prototyping services, and small volume production.

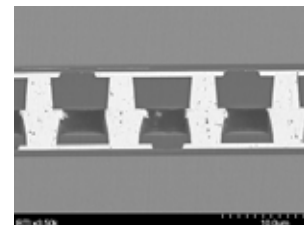
3D Process Modules

- Through-silicon via (TSV) interconnects
- Wafer thinning and temporary carrier wafer
- High-density metal-metal and polymer bonding
- Large-area multi-level metal routing

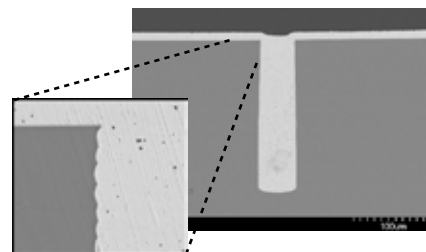


Process Technologies

RTI's 3D integration technology platform is based upon several enabling process modules. Implementations of the 3D integration process include face-to-face bonding (2 layers) and back-to-face bonding (2 layers or more).



High-density metal-metal bonding (10 µm pitch)



Through-silicon vias (TSVs)

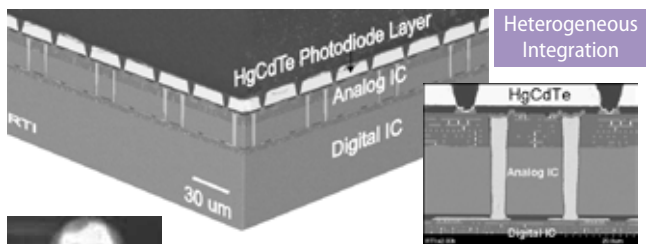


Applications

3D Integrated Circuits and 3D Packaging

By stacking silicon and/or other semiconductor layers that are, in turn, vertically interconnected by through-wafer vias, RTI provides a platform for highly integrated microsystems with increased functionality, short signal length, small size, and low power consumption. Technology demonstrations have included:

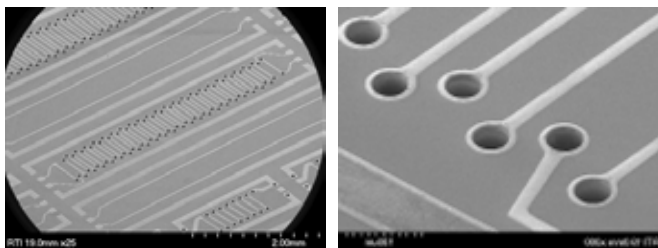
- CMOS IC wafer thinning to <20um active Si thickness
- Die bonding using either metal-to-metal or polymer bonding
- Through-wafer interconnects: 4–100 μm diameter, 8:1 aspect ratio, and densities up to $5 \times 10^5/\text{cm}^2$
- Electrical operability of 99.98% demonstrated for arrays of more than 65,000 interconnects.



3D integrated IR focal plane array and IR camera image

TSV-Enabled 3D Passives

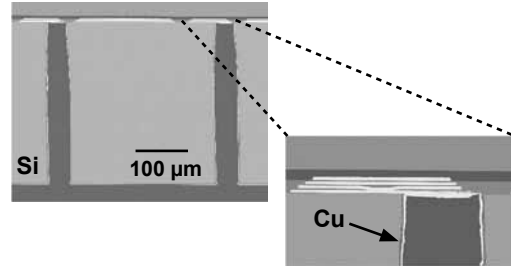
Passive 3D circuit elements, such as 3D inductors, are formed using through-silicon vias with frontside and backside metallization.



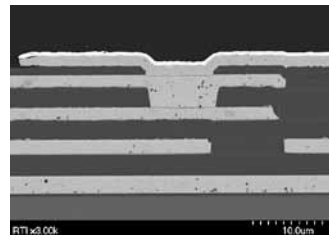
TSV-enabled 3D inductor

Silicon Interposer and Multi-Level Routing Metallization

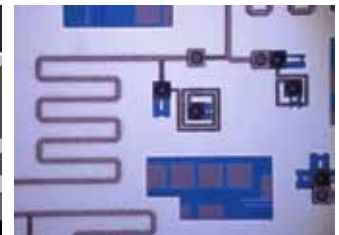
Technologies for 3D silicon interposers include wafer-scale multi-level metal interconnects for power/ground and signal routing with up to 6 levels of copper metallization, sub-10 μm line widths, and backside through-silicon vias. RTI has also demonstrated multi-level metal routing structures with spin-on BCB dielectric layers that do not require CMP.



Si interposer with MLM and backside TSV



Multi-level, large area copper metallization (5 levels, 1–4 planarized)



Multi-level routing metallization

Working with RTI

RTI is a not-for-profit company and ITAR registered organization that offers a “safe harbor” development environment to its clients. We work with a diverse base of commercial clients, government agencies, and academic institutions, supporting our clients through application-driven technology development programs, custom prototyping, and small volume production. We also partner with external organizations for joint proposals in a variety of government and defense programs, including SBIR and STTR programs.

More Information

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